

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.

L Number	Hits	Search Text	DB	Time stamp
-	326	717/140.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:39
-	0	717/1420.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:39
-	76	717/142.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:39
-	205	717/143.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:39
-	137	717/156.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:40
-	34	syntax adj analysis and (cfg or (flow adj graph))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:41
-	71	syntax adj analysis and schedul\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:41
-	25892	circuit and (time or wait\$3) near2 (restriction or minimum)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:42
-	13250	circuit and (layout or design) and compil\$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:42
-	4470	circuit same (layout or design) same (compil\$5 or synthesi\$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:43
-	1	circuit same (layout or design) same (compil\$5 or synthesi\$4) same (boundary and restriction)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:44
-	111	circuit same (layout or design) same (compil\$5 or synthesi\$4) and (boundary and restriction)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:44

-	4074	circuit same (layout or design) same (compil\$5 or synthesi\$4) and description	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:44
-	1366	circuit same (layout or design) same (compil\$5 or synthesi\$4) same description	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:44
-	334	circuit same (layout or design) same (compil\$5 or synthesi\$4) same (high-level or (high adj level) near2 description)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:45
-	168	circuit same (layout or design) same (compil\$5 or synthesi\$4) same (high-level or (high adj level) near2 description) and (cfg or (control adj flow) or nodes)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 10:46
-	9	(circuit same (layout or design) same (compil\$5 or synthesi\$4) same (high-level or (high adj level) near2 description) and (cfg or (control adj flow) or nodes) and (circuit and (time or wait\$3) near2 (restriction or minimum))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 11:05
-	12	((("6192504" "6075935" "6708325" "5966534" "6330530").pn. or "20020099756")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 11:07
-	11	((("6192504" "6075935" "6708325" "5966534" "6330530").pn. or "20020099756") and (syntax or control or (flow adj graph) or cfg or nodes or optimiz\$5 or optimis\$5 or area or wait\$3 or restriction or routing or circuit or logic or minimum or boundary or thread or schedul\$3 or priority or estimat\$3 or cost or pipeline or shar\$3 or (critical adj path) or register or solution or library or loop or memory or hardware or asic or (integrated adj circuit) or fpga or drl or reconfiguarble)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/19 11:17
-	10	5966534.URPN.	USPAT	2004/08/19 11:39


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

 Search: ☒ The ACM Digital Library ☐ The Guide

THE ACM DIGITAL LIBRARY


[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

Terms used

programmable hardware and optimizing and constraints

Found 51,184 of 140,980

Sort results by


[Save results to a Binder](#)
[Try an Advanced Search](#)
[Try this search in The ACM Guide](#)

Display results


[Search Tips](#)
☐ Open results in a new window

Results 1 - 20 of 200

Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

Best 200 shown

Relevance scale ☐ ☐ ☐ ☐ ☐

1 [Strategic directions in constraint programming](#)

Pascal Van Hentenryck, Vijay Saraswat

December 1996 **ACM Computing Surveys (CSUR)**, Volume 28 Issue 4Full text available: [pdf\(402.08 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

2 [Implementing deductive databases by linear programming](#)

Colin Bell, Anil Nerode, Raymond T. Ng, V. S. Subrahmanian

July 1992 **Proceedings of the eleventh ACM SIGACT-SIGMOD-SIGART symposium on Principles of database systems**Full text available: [pdf\(926.92 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

3 [Postpass Code Optimization of Pipeline Constraints](#)

John L. Hennessy, Thomas Gross

July 1983 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 5 Issue 3Full text available: [pdf\(1.67 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

4 [Scheduling techniques for embedded systems: An integer linear programming based approach for parallelizing applications in On-chip multiprocessors](#)

I. Kadayif, M. Kandemir, U. Sezer

June 2002 **Proceedings of the 39th conference on Design automation**Full text available: [pdf\(174.70 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

With energy consumption becoming one of the first-class optimization parameters in computer system design, compilation techniques that consider performance and energy simultaneously are expected to play a central role. In particular, compiling a given application code under performance and energy constraints is becoming an important problem. In this paper, we focus on an on-chip multiprocessor architecture and present a parallelization strategy based on integer linear programming. Given an array ...

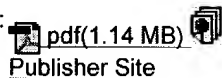
Keywords: constraint-based compilation, embedded systems, loop-Level parallelism

5 Embedded system synthesis by timing constraints solving

Krzysztof Kuchcinski

September 1997 **Proceedings of the 10th international symposium on System synthesis**

Full text available:



Publisher Site

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

This paper presents an approach to embedded system synthesis which minimizes a system cost while implementing given timing requirements. The embedded system is represented by a set of finite domain constraints defining different requirements on processes timing, system resources and interprocess communication. The assignment of processes to processors and interprocess communications to buses as well as their scheduling are then defined as an optimization problem. A prototype system, based on con ...

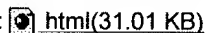
Keywords: Embedded Systems, Synthesis, Constraint Logic Programming.

6 Some challenges for constraint programming

Manuel Hermenegildo

December 1996 **ACM Computing Surveys (CSUR)**

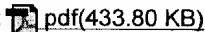
Full text available:

Additional Information: [full citation](#), [references](#)**7 TDL: a hardware description language for retargetable postpass optimizations and analyses**

Daniel Kästner

September 2003 **Proceedings of the second international conference on Generative programming and component engineering**

Full text available:

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

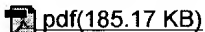
The hardware description language TDL has been designed with the goal to generate machine-dependent postpass optimizers and analyzers from a concise specification of the target processor. TDL is assembly-oriented and provides a generic modeling of irregular hardware constraints that are typical for many embedded processors. The generic modeling supports graph-based and search-based optimization algorithms. An important design goal of TDL was to achieve extendibility, so that TDL can be easily i ...

8 Optimal FPGA module placement with temporal precedence constraints

S. Fekete, E. Köhler, J. Teich

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

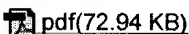
Full text available:

Additional Information: [full citation](#), [references](#), [index terms](#)**9 Partitioning of VLSI circuits and systems**

Frank M. Johannes

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available:

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

6 Generalized ILP scheduling and allocation for high-level DSP synthesis*Lucke, L.E.; Parhi, K.K.;*

Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993 , 9-12

May 1993

Pages:5.4.1 - 5.4.4

[\[Abstract\]](#) [\[PDF Full-Text \(388 KB\)\]](#) **IEEE CNF**

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE


[Membership](#) [Publications/Services](#) [Standards](#) [Conferences](#) [Careers/Jobs](#)

 Welcome
 United States Patent and Trademark Office


>> Search

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **15** of **1060766** documents.A maximum of **500** results are displayed, **50** to a page, sorted by **Relevance Descending** order.**Refine This Search:**

You may refine your search by editing the current search expression or enter a new one in the text box.

☐ Check to search within this result set
Results Key:**JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 Development of robust interconnect model based on design of experiments and multiobjective optimization**

Qiang Zhang; Liou, J.J.; McMacken, J.; Thomson, J.; Layman, P.;
 Electron Devices, IEEE Transactions on , Volume: 48 , Issue: 9 , Sept. 2001
 Pages:1885 - 1891

[\[Abstract\]](#) [\[PDF Full-Text \(181 KB\)\]](#) **IEEE JNL**
2 Multiobjective optimization of component placement on planar printed wiring boards

Queipo, N.V.; Gil, G.F.;
 Semiconductor Thermal Measurement and Management Symposium, 1997. S THERM XIII., Thirteenth Annual IEEE , 28-30 Jan. 1997
 Pages:92 - 105

[\[Abstract\]](#) [\[PDF Full-Text \(1148 KB\)\]](#) **IEEE CNF**
3 Multiobjective optimization of component placement on printed wiring boards

Queipo, N.V.; Humphrey, J.A.C.; Ortega, A.;
 Thermal Phenomena in Electronic Systems, 1996. I-THERM V., Inter-Society Conference on , 29 May-1 June 1996
 Pages:359 - 372

[\[Abstract\]](#) [\[PDF Full-Text \(1140 KB\)\]](#) **IEEE CNF**
4 MOGAC: a multiobjective genetic algorithm for hardware-software cosynthesis of distributed embedded systems

Dick, R.P.; Jha, N.K.;
 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction

on , Volume: 17 , Issue: 10 , Oct. 1998
 Pages:920 - 935

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) IEEE JNL

5 Multiobjective optimal placement of convectively cooled electronic components on printed wiring boards

Queipo, N.V.; Humphrey, J.A.C.; Ortega, A.;

Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on] , Volume: 21 , Issue: 1 , March 1998
 Pages:142 - 153

[\[Abstract\]](#) [\[PDF Full-Text \(260 KB\)\]](#) IEEE JNL

6 Sensitivity analysis of iterative design processes

Johnson, E.W.; Brockman, J.B.; Vigeland, R.;

Computer-Aided Design, 1996. ICCAD-96. Digest of Technical Papers., 1996 IEEE/ACM International Conference on , 10-14 Nov. 1996
 Pages:142 - 145

[\[Abstract\]](#) [\[PDF Full-Text \(356 KB\)\]](#) IEEE CNF

7 Pareto optimal nonlinear filters for image enhancement

Shcherbakov, M.A.;

Image Processing, 1996. Proceedings., International Conference on , Volume 1 , 16-19 Sept. 1996
 Pages:769 - 772 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(488 KB\)\]](#) IEEE CNF

8 Multimedia ASIP SoC codesign based on multicriteria optimization

J-Horng Jeng; Feipei Lai; Naroska, E.; Schwiegelshohn, U.;

Consumer Electronics, 2001. ICCE. International Conference on , 19-21 June
 Pages:342 - 343

[\[Abstract\]](#) [\[PDF Full-Text \(164 KB\)\]](#) IEEE CNF

9 On the selection of parts and processes during design of printed circuit board assemblies

Ball, M.O.; Baras, J.S.; Bashyam, S.; Karne, R.K.; Trichur, V.S.;

Emerging Technologies and Factory Automation, 1995. ETFA '95, Proceedings 1995 INRIA/IEEE Symposium on , Volume: 3 , 10-13 Oct. 1995
 Pages:241 - 248 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(400 KB\)\]](#) IEEE CNF

10 The design of low sensitivity digital filters using multi-criterion optimization strategies

DeBrunner, V.E.;

Acoustics, Speech, and Signal Processing, 1992. ICASSP-92., 1992 IEEE International Conference on , Volume: 4 , 23-26 March 1992
 Pages:317 - 320 vol.4

[\[Abstract\]](#) [\[PDF Full-Text \(284 KB\)\]](#) IEEE CNF

11 Synthesis of custom interleaved memory systems

Song Chen; Postula, A.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 8 , Issue: 1 , Feb. 2000

Pages:74 - 83

[\[Abstract\]](#) [\[PDF Full-Text \(196 KB\)\]](#) IEEE JNL

12 Control of multirate synchronous streams in hybrid TDM access networks

Bolla, R.; Davoli, F.;

Networking, IEEE/ACM Transactions on , Volume: 5 , Issue: 2 , April 1997

Pages:291 - 304

[\[Abstract\]](#) [\[PDF Full-Text \(1404 KB\)\]](#) IEEE JNL

13 Design optimization of a high-speed permanent magnet machine with the VEKOPT algorithm

Schatzer, Ch.; Binder, A.;

Industry Applications Conference, 2000. Conference Record of the 2000 IEEE , Volume: 1 , 8-12 Oct. 2000

Pages:439 - 444 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(476 KB\)\]](#) IEEE CNF

14 Optimisation problems for dynamic concurrent task-based systems

Verkest, D.; Yang, P.; Wong, C.; Marchal, P.;

Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM International Conference on , 4-8 Nov. 2001

Pages:265 - 268

[\[Abstract\]](#) [\[PDF Full-Text \(227 KB\)\]](#) IEEE CNF

15 Statistical approach for improving manufacturing yield in advanced fabrication

Carlson, A.C.; Sundaran, S.L.;

Advanced Semiconductor Manufacturing Conference and Workshop, 1991. AS 91 Proceedings. IEEE/SEMI 1991 , 21-23 Oct. 1991

Pages:25 - 29

[\[Abstract\]](#) [\[PDF Full-Text \(364 KB\)\]](#) IEEE CNF

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

Welcome
United States Patent and Trademark Office

» Se.

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **5** of **1060766** documents.A maximum of **500** results are displayed, **50** to a page, sorted by **Relevance Descending** order.**Refine This Search:**

You may refine your search by editing the current search expression or enter a new one in the text box.

☐ Check to search within this result set
Results Key:**JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 3D exploration of software schedules for DSP algorithms***Teich, J.; Zitzler, E.; Bhattacharyya, S.S.;*

Hardware/Software Codesign, 1999. (CODES '99) Proceedings of the Seventh International Workshop on , 3-5 May 1999

Pages:168 - 172

[\[Abstract\]](#)
[\[PDF Full-Text \(436 KB\)\]](#)
IEEE CNF**2 Task concurrency management methodology summary***Chun Wong; Marchal, P.; Peng Yang; Prayati, A.; Cossement, N.; Catthoor, F. Lauwereins, R.; Verkest, D.; De Man, H.;*

Design, Automation and Test in Europe, 2001. Conference and Exhibition 200 Proceedings , 13-16 March 2001

Pages:813

[\[Abstract\]](#)
[\[PDF Full-Text \(64 KB\)\]](#)
IEEE CNF**3 Multimedia ASIP SoC codesign based on multicriteria optimization***J-Horng Jeng; Feipei Lai; Naroska, E.; Schwiegelshohn, U.;*

Consumer Electronics, 2001. ICCE. International Conference on , 19-21 June Pages:342 - 343

[\[Abstract\]](#)
[\[PDF Full-Text \(164 KB\)\]](#)
IEEE CNF**4 MOGAC: a multiobjective genetic algorithm for hardware-software cosynthesis of distributed embedded systems***Dick, R.P.; Jha, N.K.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 17 , Issue: 10 , Oct. 1998

Pages:920 - 935

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) **IEEE JNL**

5 RS-FDRA: a register sensitive software pipelining algorithm for embedded VLIW processors

Akturan, C.; Jacome, M.F.;

Hardware/Software Codesign, 2001. CODES 2001. Proceedings of the Ninth International Symposium on , 25-27 April 2001

Pages:67 - 72

[\[Abstract\]](#) [\[PDF Full-Text \(696 KB\)\]](#) **IEEE CNF**

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved